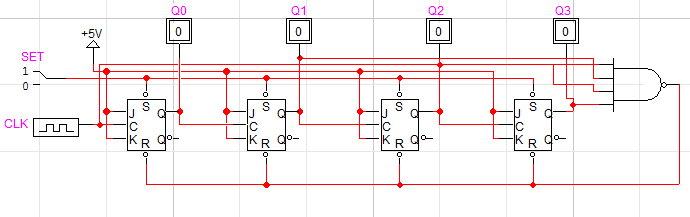
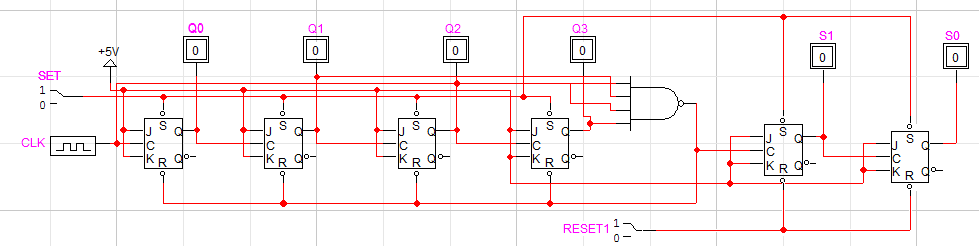
**DLD Lab 14**

Q1) Design a 4 bit asynchronous counter using JK flip flop which counts from 0-14.

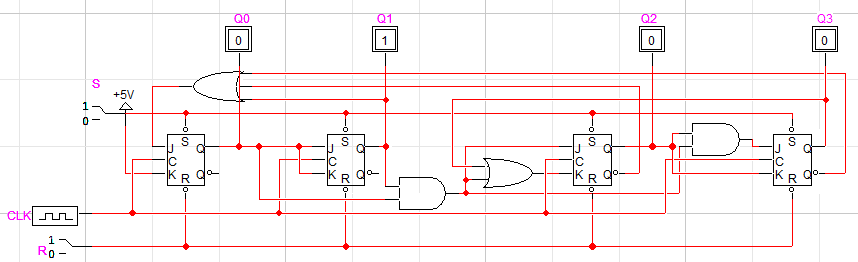


Q2) Design a 4 bit asynchronous counter using JK flip flop which counts from 0-14 and at each

time counter resets to 0 then increase count in other 2 bit counter by 1.



Q3) Design a 4 bit Synchronous counter using JK flip flop which counts from 0-12.



Q4) Design a 4 bit Synchronous counter using JK flip flop which counts from 10-0.

